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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/956,903	09/21/2001	Thomas D. Fletcher	2207/11270	2661
23838	7590	05/19/2005	EXAMINER	
KENYON & KENYON 1 BROADWAY NEW YORK, NY 10004			DO, CHAT C	
		ART UNIT		PAPER NUMBER
				2193

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/956,903	FLETCHER, THOMAS D.
	Examiner Chat C. Do	Art Unit 2193

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 10 January 2005.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-14, 16-21 and 23-31 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) 20, 21, 23 and 24 is/are allowed.
 6) Claim(s) 1-14, 25-31 is/are rejected.
 7) Claim(s) 16-19 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date 11/18/02.

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 01/10/2005.
2. Claims 1-14, 16-21, and 23-31 are pending in this application. Claims 1, 4, 10, 20, and 25 are independent claims. In Amendment, claims 15 and 22 are cancelled; and claim 31 is added. This Office Action is made final.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-14 and 25-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Winters (U.S. 6,292,818).

Re claim 1, Winters discloses in Figures 3 and 6 an apparatus comprising a symmetric differential domino (col. 3 lines 22-24) carry generate circuit (Figure 6) having true inputs (e.g. A1H, B1H, ...) and compliment inputs (e.g. A1L, B1L...) which both have a load (e.g. inherently there must be a load/current exist on these input signal), wherein the load for the true inputs is equal to the load for the compliment inputs (Figure 6).

Re claim 2, Winters further discloses in Figures 3 and 6 the circuit also has a true carry generate output (24 as CAR) and a compliment carry generate output (the other output) which both have an output drive strength (e.g. for signaling other circuit or component), and wherein the output drive strength for true output is the same as the output drive strength for compliment output (Figure 6).

Re claim 3, Winters further discloses in Figures 3 and 6 the circuit further comprises: a first evaluation block (transistors that have A1H, B1H, and C1H as inputs) having a plurality of transistors, wherein a number p of transistors are connected in a parallel relationship (e.g. transistor of A1H and C1H) and a number of transistors are connected in a serial relationship (e.g. transistor of A1H and B1H); and a second evaluation block (transistors that have A1L, B1L, and C1L as inputs) having a plurality of transistors, wherein in the second evaluation block p transistors are connected in a parallel relationship (e.g. transistor of A1L and C1L as A1L) and transistors are connected in a serial relationship (e.g. transistor of A1L and B1L).

Re claim 4, Winters discloses in Figures 3 and 6 an apparatus comprising a differential domino carry generate circuit having a first evaluation block of switches (transistors that have A1H, B1H, and C1H as inputs) and a second evaluation block of switches (e.g. transistors that have A1L, B1L, and C1L as inputs), wherein the first evaluation block and second evaluation block each have the same number switches connected in parallel and each have the same number of transistors connected in series (e.g. they are mirror) and wherein the circuit also has a true carry generate output and a compliment carry generate output which both have an output drive strength, and therein

the output drive strength for true output is the same as the output drive strength for compliment output (e.g. capable for signaling other circuit or component).

Re claim 5, Winters further discloses in Figures 3 and 6 the switches in the first evaluation block and second evaluation block are N-channel metal-oxide semiconductor (NMOS) transistors (Figure 6).

Re claim 6, Winters further discloses in Figures 3 and 6 corresponding transistors in the first evaluation block and second evaluation block are the same size (they are mirror and total transistors in each block is 6).

Re claim 7, Winters further discloses in Figures 3 and 6 the apparatus further comprises cross-coupled P-channel metal-oxide semiconductor (PMOS) keeper transistors (transistors that poll VDD).

Re claim 8, Winters further discloses in Figures 3 and 6 the differential domino carry generate circuit is a first stage in a carry look-ahead adder (abstract and Figure 3).

Re claim 9, Winters further discloses in Figures 3 and 6 the differential domino carry generate circuit is a group generate gate (abstract).

Re claim 10, Winters discloses in Figures 3 and 6 an apparatus comprising: a first output to provide a pre-charge value (26) during a pre-charge phase and a true carry generate value driving an evaluation phase (transistors that have A1H, B1H, and C1H as inputs); a second output to provide the pre-charge value (25) during the pre-charge phase and the compliment of the true carry generate true during the evaluation phase (transistors that have A1L, B1L, and C1L as inputs); a current input (VDD); a first evaluation block (transistors that have A1H, B1H, and C1H as inputs) connected to the

current input and the first output and having a plurality of transistors, wherein a number of transistors are connected in a parallel relationship and a number of transistors are connected in a serial relationship, a first transistor with a drain connected to the second output, a second transistor with a drain connected to the source of the first transistor and a source connected to the current input, a third transistor with a drain connected to the second output, a fourth transistor with a drain connected to the source of the third transistor and a source connected to the current input, and a fifth transistor with a drain connected to the source of the fourth transistor and a source connected to the second output (e.g. series model of transistors as seen in Figure 6 with transistors that have A1H, B1H, and C1H as inputs); and a second evaluation block connected to the current input and the second output and having a plurality of transistors, wherein the second evaluation block (transistors that have A1L, B1L, and C1L as inputs) has the same number of transistors connected in a parallel relationship as the first evaluation block and the same number of transistors connected in a serial relationship as the first evaluation block (left portion in Figure 6 is mirror the right portion of Figure 6).

Re claim 11, Winters further discloses in Figures 3 and 6 the output drive strength for the first output is the same as the output drive strength for the second output (same VDD in the pre-charge in Figure 6).

Re claim 12, Winters further discloses in Figures 3 and 6 the circuit further comprises a clock input to receive a clock having precharge and evaluation phases (e.g. 25 or 26 in Figure 6).

Re claim 13, Winters further discloses in Figures 3 and 6 the current input is a transistor having a source node connected to ground (e.g. indirectly with GND in Figure 6) and a gate connected to the clock input (e.g. 25).

Re claim 14, Winters further discloses in Figures 3 and 6 the gate of each transistor in the first evaluation block (transistors that have A1H, B1H, and C1H as inputs) is connected to one of a set of true inputs and the gate of each of the transistors in the second evaluation block (transistors that have A1L, B1L, and C1L as inputs) is connected to one of a set of compliment inputs, and wherein the load for the true inputs is the same as the load for the compliment inputs (Figure 6).

Re claim 25, it is a method claim of claim 10. Thus, claim 25 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 26, Winters further discloses in Figures 3 and 6 the first evaluation block and second evaluation block have corresponding stacks that have the same number of transistors (for each the total transistors is 6).

Re claim 27, Winters further discloses in Figures 3 and 6 the method receiving a clock (C1L and C1H) having a pre-charge phase (transistors at 25 and 26) and an evaluation phase (Figure 6); providing pre-charge values at the first output and at the second output during pre-charge phase; and providing the compliment carry generate value at the first output and the compliment carry generate value at the second output during the evaluation phase (output of Figure 6).

Re claim 28, Winters further discloses in Figures 3 and 6 the method further comprises preventing current from passing through the current input during the precharge

phase and enabling current to pass through the current input during the evaluation phase (e.g. 25 and 26).

Re claim 29, Winters further discloses in Figures 3 and 6 the method further comprises: providing the output from the first evaluation block to a keeper (left VDD power source in Figure 6); providing the output from the second evaluation block to a keeper (right VDD power source in Figure 6); and providing the carry generate true output (output of 25) and carry generate compliment output (output of 26) during the evaluation phase based upon output from the first evaluation block (High inputs block), second evaluation block (Low input block), and the keeper (two VDD transistors).

Re claim 30, Winters further discloses in Figures 3 and 6 the inputs received and outputs provided are symmetrical (the left portion is mirror the right portion as seen in Figure 6).

Re claim 31, Winters further discloses in Figures 3 and 6 that the first evaluation block has three stacks of transistors (e.g. transistors for receiving A1H, B1H, and C1H in Figure 6), and wherein the second evaluation block has three stacks of transistors (e.g. transistors fro receiving A1L, B1L, and C1L in Figure 6).

Allowable Subject Matter

5. Claims 16-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
6. Claims 20-21 and 23-24 are allowed.

Response to Arguments

7. Applicant's arguments filed 01/10/2005 have been fully considered but they are not persuasive.

a. The applicant argues in page 13 for claims 1-4 that the cited reference does not disclose or suggest the any characteristics of (1) the load for any inputs (2) the output drive strength for any outputs as cited in the claimed invention.

The examiner respectfully submits that the cited reference clearly discloses in Figure 6 the true inputs (e.g. A1H, B1H, and C1H) and the complement inputs (e.g. A1L, B1L, and C1L). These inputs must have a load as the input of A and B operand respectively in Figure 3. In addition, the load of true inputs is equal to the load of their complement because they are complement to each other.

Inherently, the output must have signal strength to identify or drive other circuit/component.

b. The applicant argues in page 14 for claims 10-14 that the cited reference does not disclose or suggest a first evaluation block that comprises "a fourth transistor with a drain connected to the source of the third transistor and a source connected to the current input, and a fifth transistor with a drain connected to the second output and a source connected to the drain of the fourth transistor" as cited in the claimed invention.

The examiner respectfully submits that the cited reference discloses in Figure 6 with the first, second, third, fourth, and fifth transistors as transistors for receiving

A1H, B1H, A1L, B1L and A1H respectively as claimed in the claimed structure wherein a fourth transistor (e.g. transistor on the right for receiving B1L) with a drain connected to the source of the third transistor (e.g. transistor on the left for receiving A1L) and a source connected to the current input, and a fifth transistor (e.g. transistor for receiving A1H) with a drain connected to the second output (e.g. either 25/26 as EVAL) and a source connected to the drain of the fourth transistor"

c. The applicant argues in page 15-16 for claims 25-30 that the cited reference does not disclose or suggest a method that includes processing compliment input values at a second evaluation block to provide a carry generate value, or processing true input values at a first evaluation block to provide the compliment of a carry generate value.

The examiner respectfully submits that the cited reference discloses in Figure 6 particularly part 21B a method that includes processing compliment input values at a second evaluation block to provide a carry generate value (e.g. 23 for carry as in 21A), or processing true input values at a first evaluation block to provide the compliment of a carry generate value (e.g. 22 for carry as in 21A because the structure for sum and carry are mirror).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

May 9, 2005



TODD INGBERG
PRIMARY EXAMINER